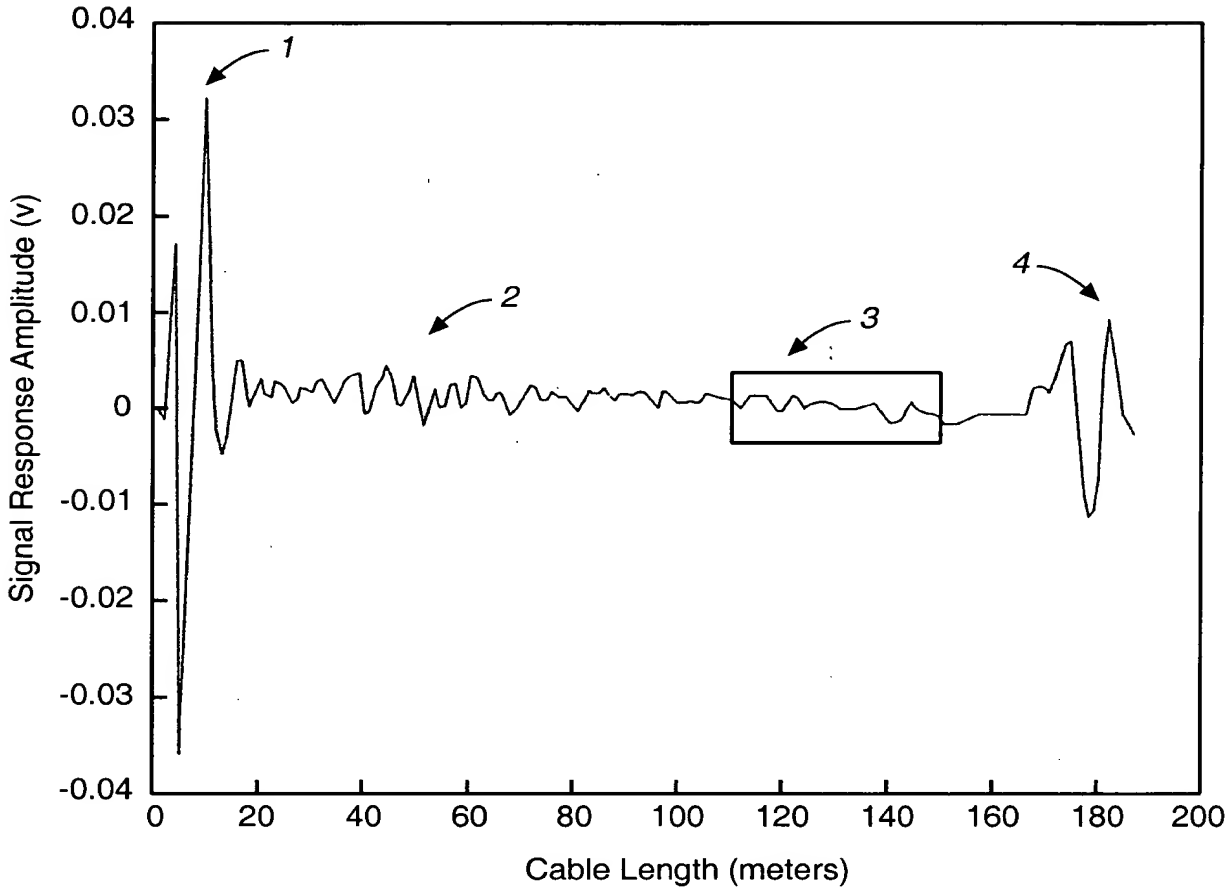
0.04
0.03
0.02
0.01
0
-0.01
-0.02
-0.03
-0.04
Signal Response Amplitude (v)
0
20
40
60
80
100
120
140
160
180
200
Cable Length (meters)
1
2
3
4

FIG._1

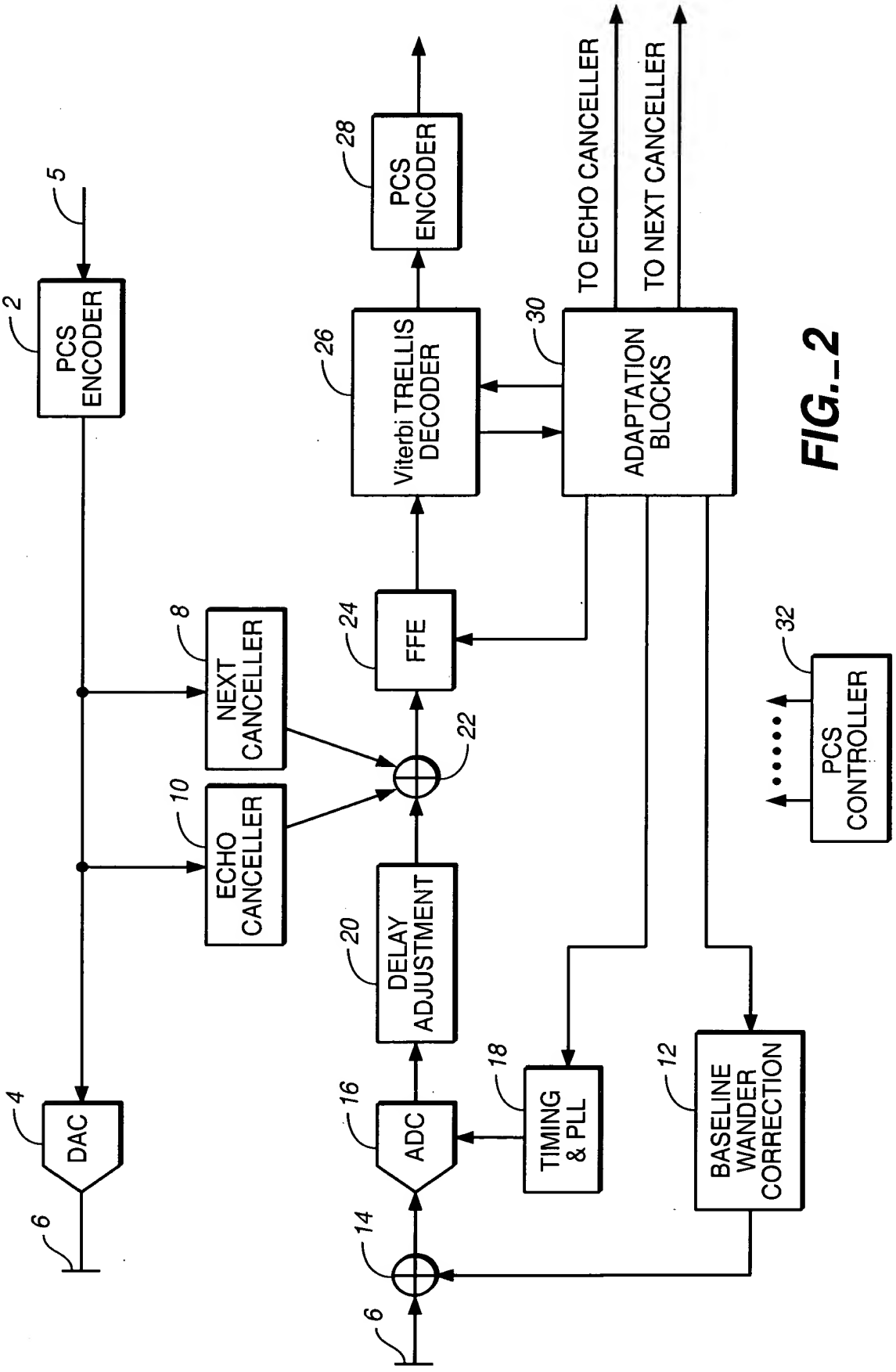

FIG._2

20502D" 06T9760

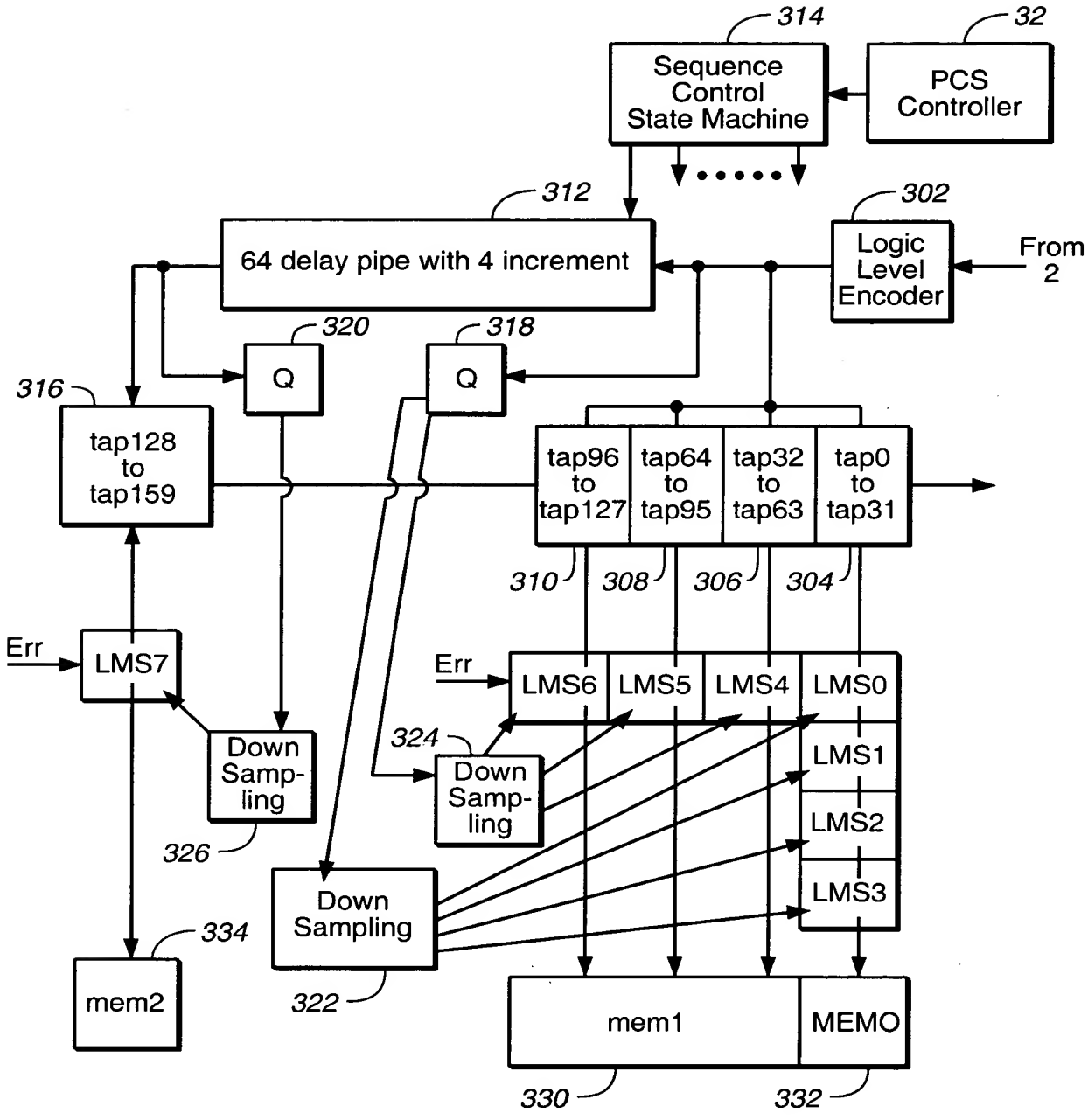
314
32
Sequence Control State Machine
PCS Controller
312
302
64 delay pipe with 4 increment
Logic Level Encoder
From 2
320
318
Q
Q
316
tap128 to tap159
tap96 to tap127
tap64 to tap95
tap32 to tap63
tap0 to tap31
310
308
306
304
Err
LMS7
Err
LMS6
LMS5
LMS4
LMS0
LMS1
LMS2
LMS3
324
Down Samp-ling
Down Samp-ling
326
Down Sampling
334
mem2
322
mem1
MEMO
330
332

FIG._3

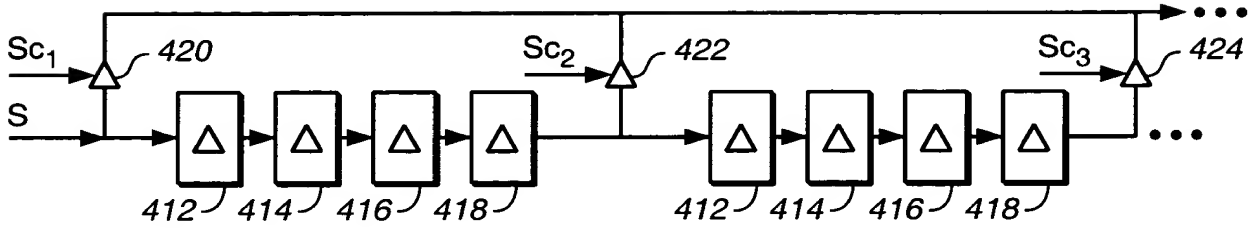
Sc1
420
Sc2
422
Sc3
424
S
412
414
416
418
412
414
416
418

FIG._4

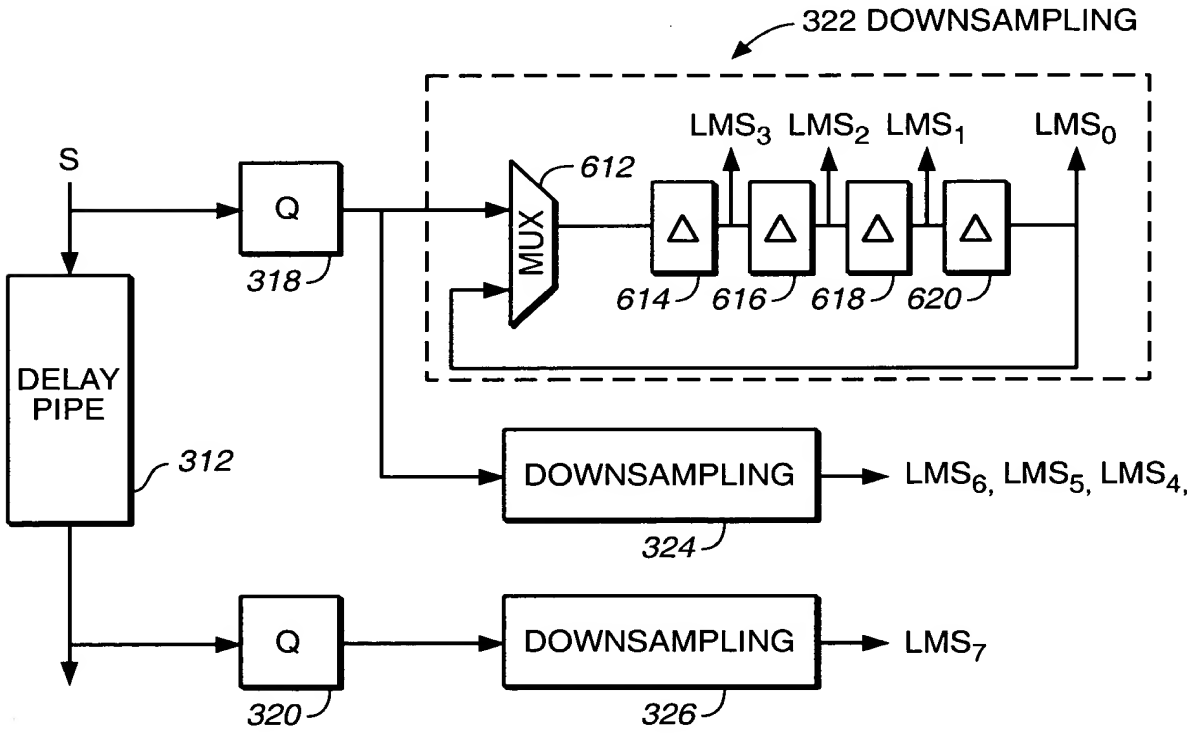
322 DOWNSAMPLING
LMS3 LMS2 LMS1 LMS0
S
Q
318
612
MUX
614
616
618
620
DELAY PIPE
312
DOWNSAMPLING
LMS6, LMS5, LMS4,
324
Q
320
DOWNSAMPLING
LMS7
326

FIG._6

20040106759

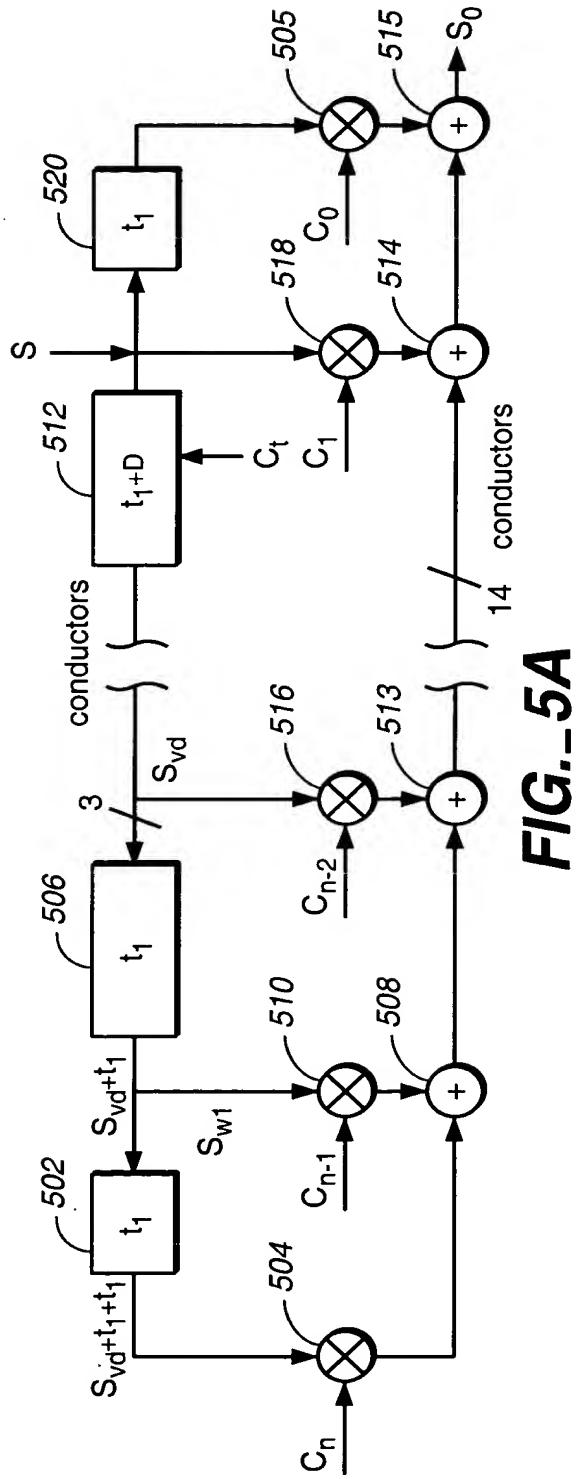

FIG._5A

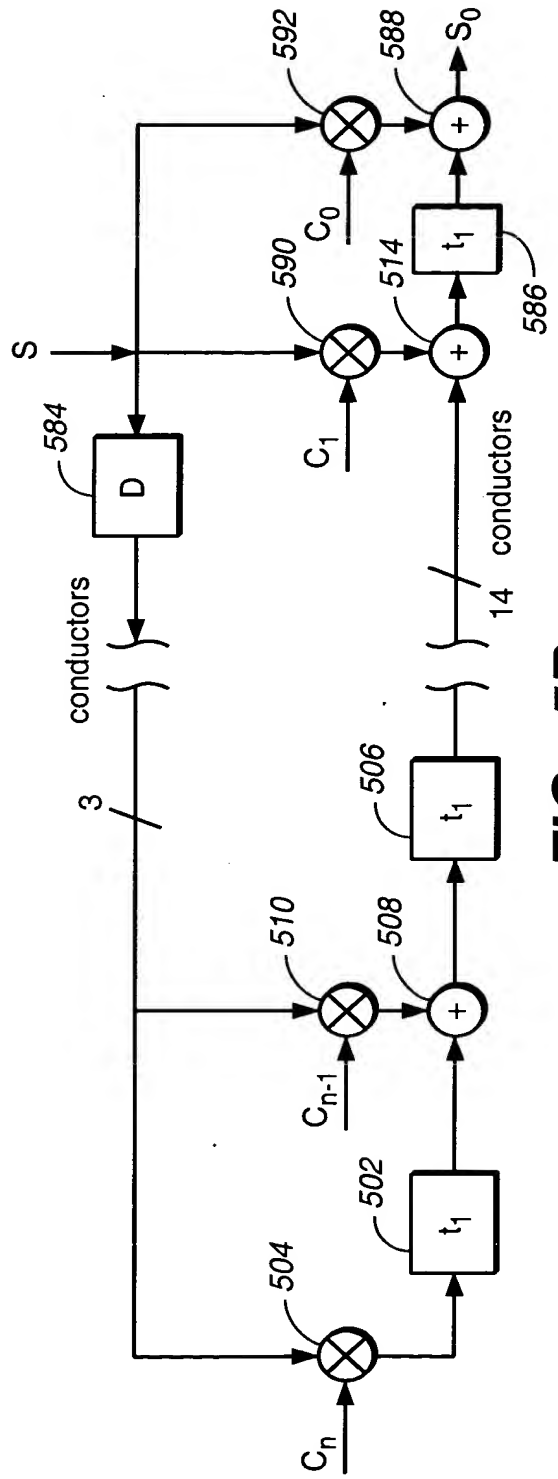

FIG._5B

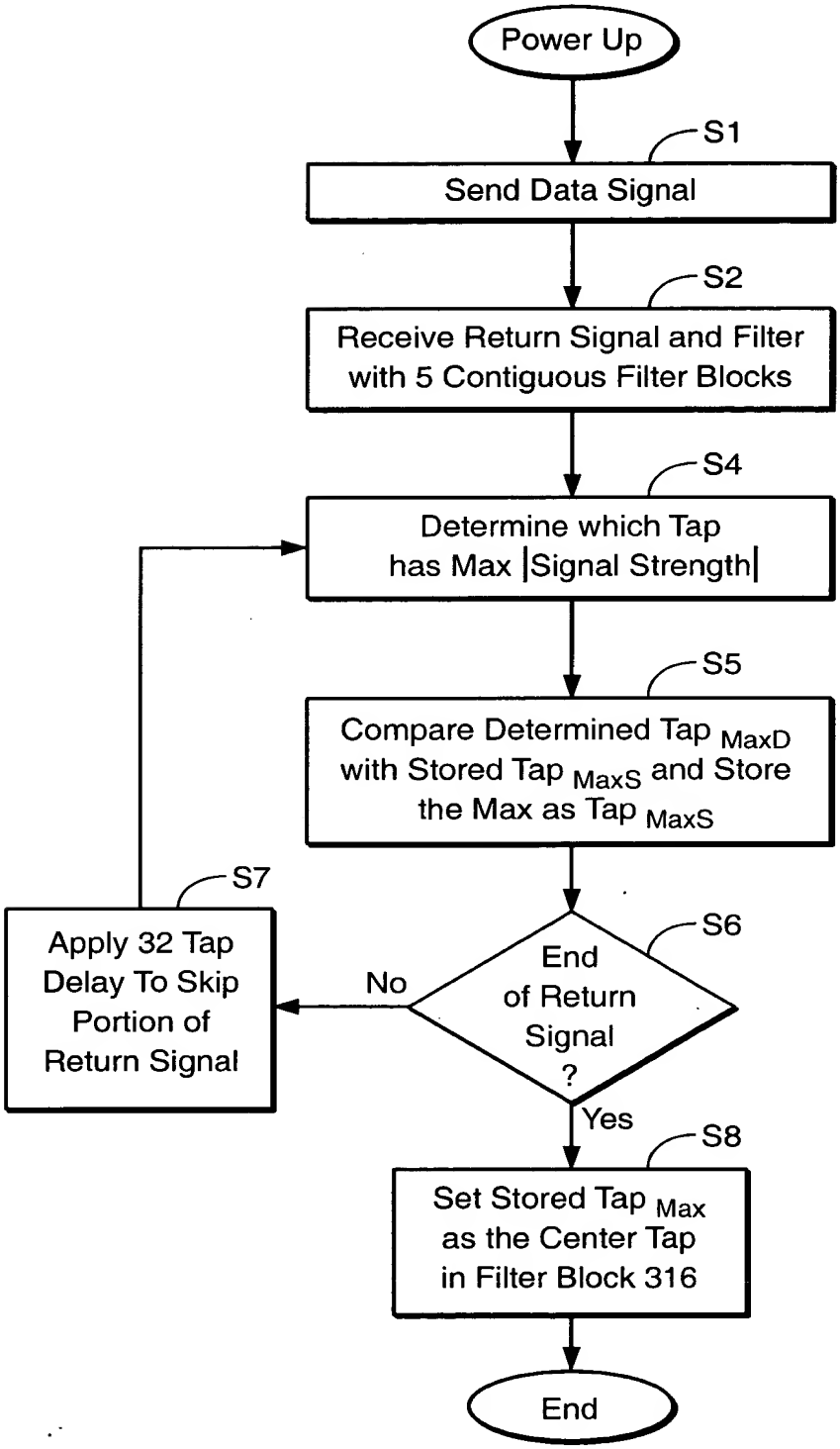
Power Up
S1
Send Data Signal
S2
Receive Return Signal and Filter with 5 Contiguous Filter Blocks
S4
Determine which Tap has Max |Signal Strength|
S5
Compare Determined Tap MaxD with Stored Tap MaxS and Store the Max as Tap MaxS
S6
End of Return Signal ?
No
S7
Apply 32 Tap Delay To Skip Portion of Return Signal
Yes
S8
Set Stored Tap Max as the Center Tap in Filter Block 316
End

FIG._7

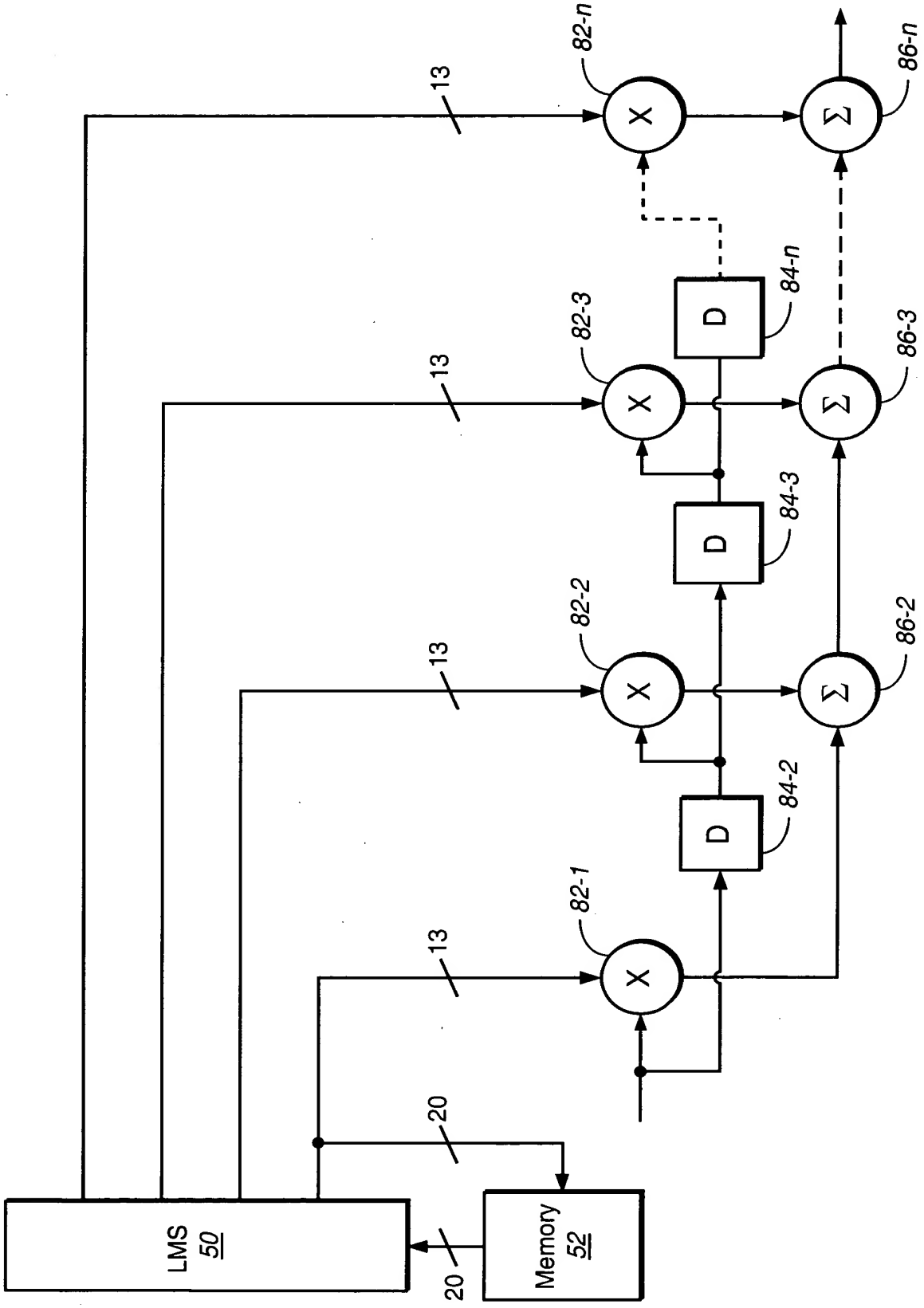
LMS
50
Memory
52
20
20
13
13
13
13
82-n
82-3
82-2
82-1
84-n
84-3
84-2
86-n
86-3
86-2
X
Σ
D

FIG._8

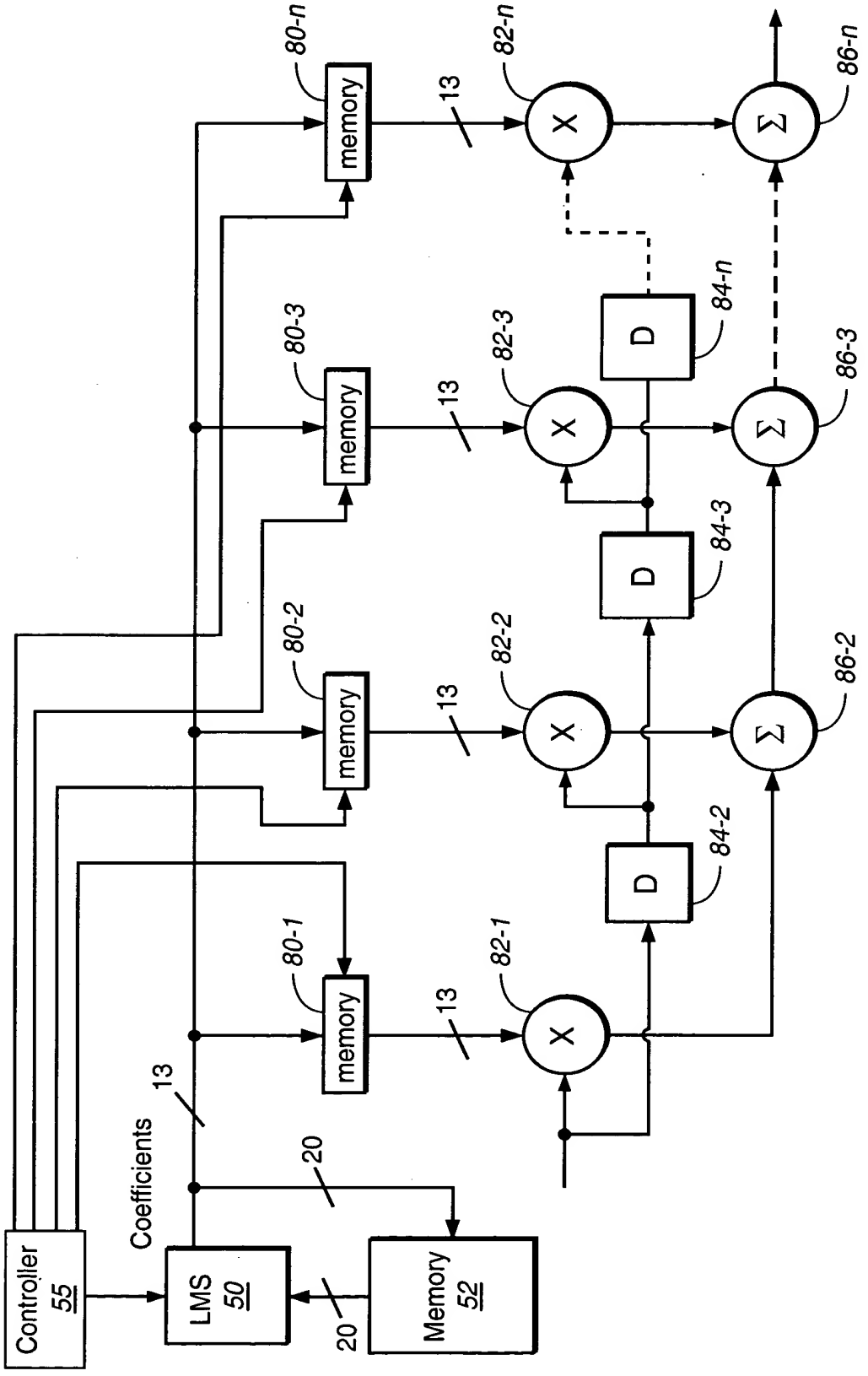

FIG._9

20502.0" 06T9750

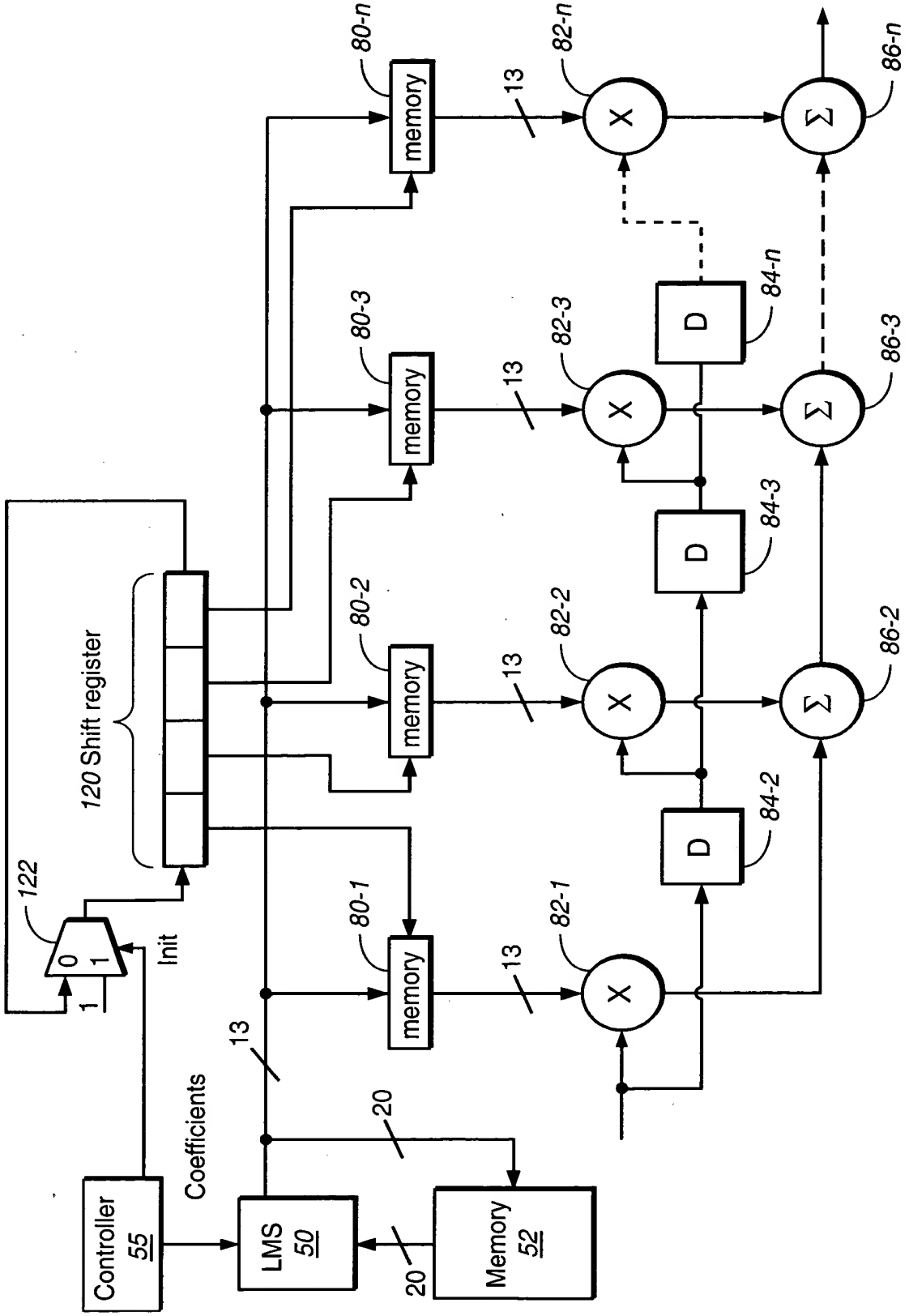
80-n
memory
13
82-n
X
Σ
86-n
84-n
D
80-3
memory
13
82-3
X
Σ
86-3
84-3
D
80-2
memory
13
82-2
X
Σ
86-2
84-2
D
80-1
memory
13
82-1
X
120 Shift register
122
0
1
1
Init
13
Coefficients
20
Controller 55
LMS 50
20
Memory 52

FIG._10

09764190 "070502

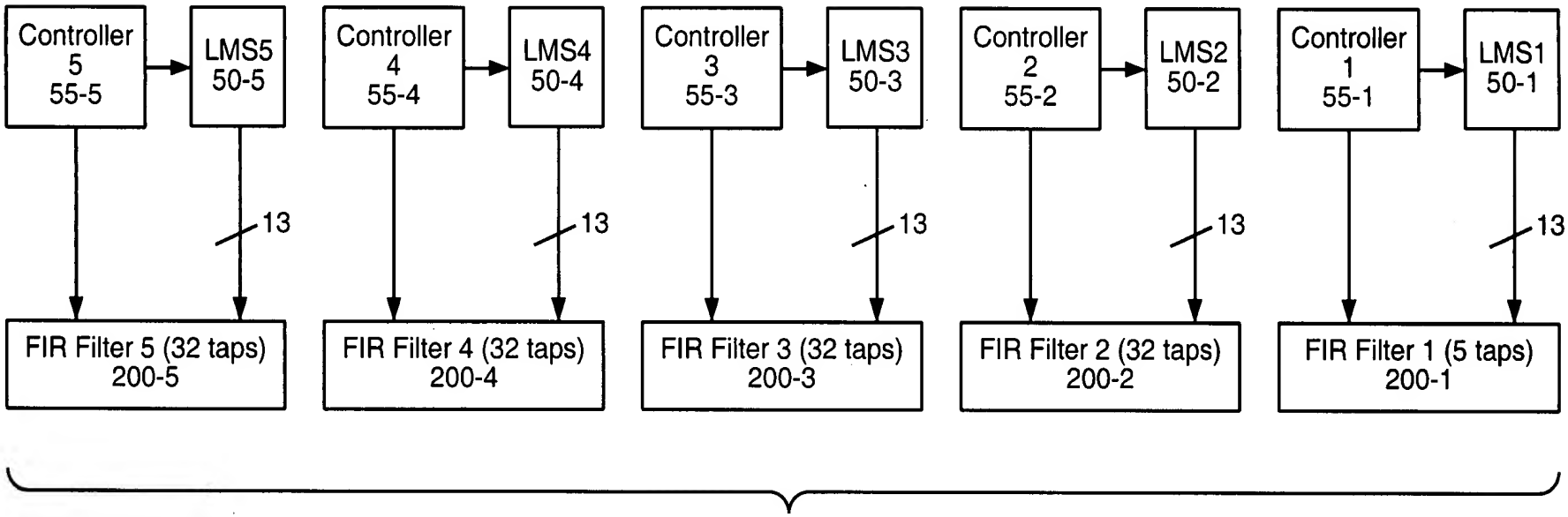

FIG._11